

**DATA
MACHINES
INC.**

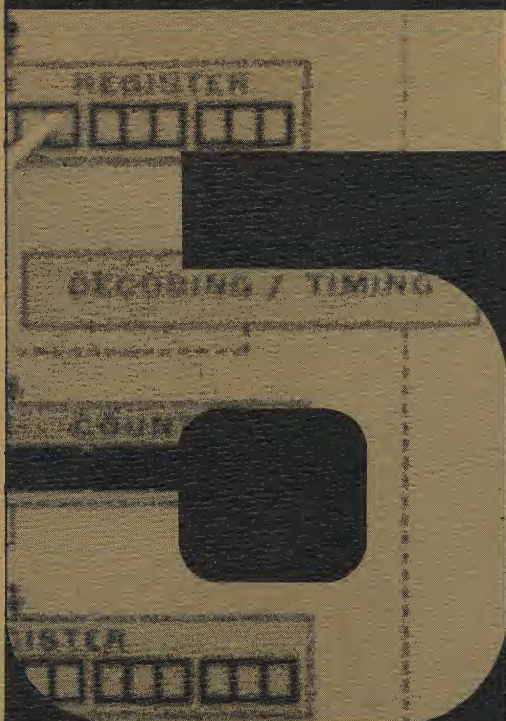
SERIES



6F5 DIGITAL



COMPUTER



TRAINER

FOR INSTRUCTION IN DIGITAL COMPUTER TECHNOLOGY

The 6F5 Trainer was developed by DMI for the U.S. Army Participation Group at the Naval Training Devices Center, Port Washington, New York, to be used in Digital Computer Technology Courses at the U. S. Army Air Defense School, Fort Bliss.

6F5 DIGITAL COMPUTER TRAINER SERIES

For Instruction In

**COMPUTER DESIGN
COMPUTER ORGANIZATION
COMPUTER OPERATION
COMPUTER MAINTENANCE
COMPUTER PROGRAMMING
INFORMATION SYSTEMS
CONTROL SYSTEMS**

**Principles
Demonstrated
By 6F5**

Computer Technology

Computer Organization
Computer Operation
Addressing techniques
Arithmetic Algorithms
Control algorithms
Interrupt operation
Time share operation
Input/output operation
Input/output interfacing

Computer Programming

Programming techniques
Machine language
Assemblers
Compilers
Executive systems
Program Debugging
Diagnostic programming

Computer Maintenance

Effects of computer malfunctions
Maintenance programs
Programming for fault isolation
Troubleshooting techniques
Maintenance documentation
Digital logic

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students' rapid comprehension in computer design, operation, programming, and maintenance.

The computer (DATA 620) is internally and externally designed for ease of operation, understanding, and programming. The mechanical layout is grouped by functions, critical signals are color coded, all control points are contained on the maintenance panel, operation and control are displayed on the control panel and the electronics are all easily accessible. The classroom display panel is operated from the computer and demonstrates the flow of data and instructions through each step of computer operation. The external keyboard control unit provides manual control of all micro-steps in the computer. The micro-steps under manual control can be sequenced to demonstrate and prove arithmetic and control designs. This booklet discusses the elements of the 6F5 series with some of the more important details as they pertain to instruction in computer technology.

Special Features

Classroom Display
The four-by-seven foot DISPLAY contains a color-coded computer organization diagram. The students have a visual demonstration of each event during the execution of a computer instruction or program. The cycle, phase, and mode of operations are presented with register contents and information flow.

Central Processor
The central processor is a full-scale general-purpose digital computer optimized for educational use. It contains and demonstrates the power and capability of present-day computing equipment. The mechanical design includes many features which aid the student in understanding the concepts of a computer, and aid the instructor in presenting computer topics. The processor is modular and can be easily expanded to include peripheral devices.

Interrupt
The processor contains a program interrupt. Many current and future

computer applications involve real-time or time-shared operation. The interrupt facility permits the demonstration and exploration of the use of interrupt in those applications.

**Indexing,
Indirect Addressing,
Relative Addressing**
All of these addressing techniques are commonly used in contemporary computing equipment. The presence of these in the processor permit the student to understand and be experienced in the concepts of addressing computer information and programs. The processor also includes direct addressing and immediate addressing. Byte addressing and extended addressing are available as processor options.

Micro-Exec (optional)
The basic design of the central processor includes provisions for adding an external control unit which can control over forty micro-steps. The external control unit defines the function of the registers, directs communication paths, directs the I/O unit, memory, and the arithmetic unit. This comprehensive control enables arithmetic and control algorithms to be defined and manually sequenced. Micro-Exec enables the 6F5 to serve as a training device in computer design courses.

Software
The basic software includes Assembler, Library Subroutines, AID, Maintain, Diagnostics, and FORTRAN. The software is modular, compatible across systems, and open ended. It is designed to enable the student to add characteristics to the programming systems. The basic software satisfies the needs of a general course in programming. The structure of the systems software is course material for upper-divisional system programming courses.

Installation
The system mounts in a standard 19-inch cabinet, and requires no air conditioning, sub-flooring, special wiring or other site preparation. The equipment can be mounted on casters for moving from laboratory to classroom, etc.

Application

The application of digital computers throughout the military, government, industry, business and specialized professions is increasing at a rapid rate. This rate of increase is requiring an even greater increased number of people educated and trained in computer technology.

Academic organizations throughout the world are assuming the responsibility of educating and training people in the utilization and advancement of this technology. Government and industry are providing personnel training and retraining. These activities are still not keeping up with the requirements. The 6F5 series has been developed as an aid in meeting this need.

The students' rapid comprehension of computer technology requires classroom and laboratory training and demonstration equipment. The 6F5 series is a modular set of equipment from which specific items can be selected to satisfy general or specialized curriculum needs. The computer elements and peripheral input/output devices are items of the DATA 620 series digital computer. The classroom display and keyboard control are 6F5 series options. Software, training, and documentation are provided with the equipment. The equipment contains the capability of present-day business, scientific, and real-time digital computers. The equipment has been specifically designed for the

students' rapid comprehension in computer design, operation, programming, and maintenance.

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Software

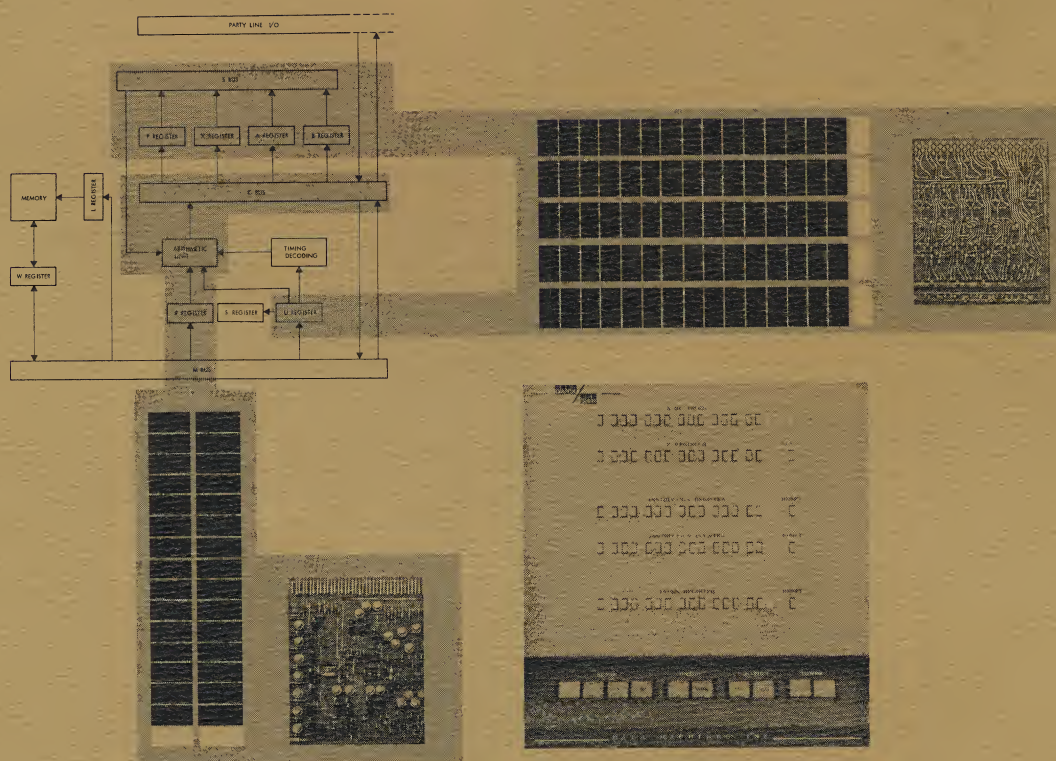
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Bit Slice

The circuit board layout is unique using a "Bit-slice" layout. "Bit-slice" is a technique whereby all the arithmetic unit and operational register circuits associated with one bit are packaged on two cards which are mounted vertically and are in a one-to-one correspondence with the bit positions on the control panel. This technique also simplifies expansion of the trainer from a 16-bit to an 18-bit configuration, allows increased component density, simplifies wiring, lowers spares requirements, and permits bit-by-bit front panel checkout of more than 75 percent of the computers' active circuits.



MICRO-EXEC

MICRO-EXEC (Optional) is a technique with which the student or instructor has the option of externally combining and sequencing the processor micro-functions to perform a complex macro-function. Over 40 micro-function control lines are made available to the user. These control functions include the micro-steps normally controlled by the processor control unit and other specially designed into the processor organization. They control memory, arithmetic unit, control unit, all registers, I/O and communication networks. The memory can be operated in the Read/Modify/Write, Read/Write, Clear/Write, and half-cycle read or write modes. The external control can operate the

micro-steps as fast as five every 900 nano-seconds. The clock synchronizes the micro-step operations.

MICRO-EXEC can be used to implement many types of algorithms. Typical functions are: convolutions, coordinate transformations, trigonometric, double precision arithmetic, floating point arithmetic, square root, limit checking, etc. MICRO-EXEC gives students a "feel" for the computer's fundamental operations at the flip-flop level. Elementary or complex functions can be implemented with the MICRO-EXEC keyboard and made accessible to the student for step-by-step manipulation.

6F5 Series Equipment

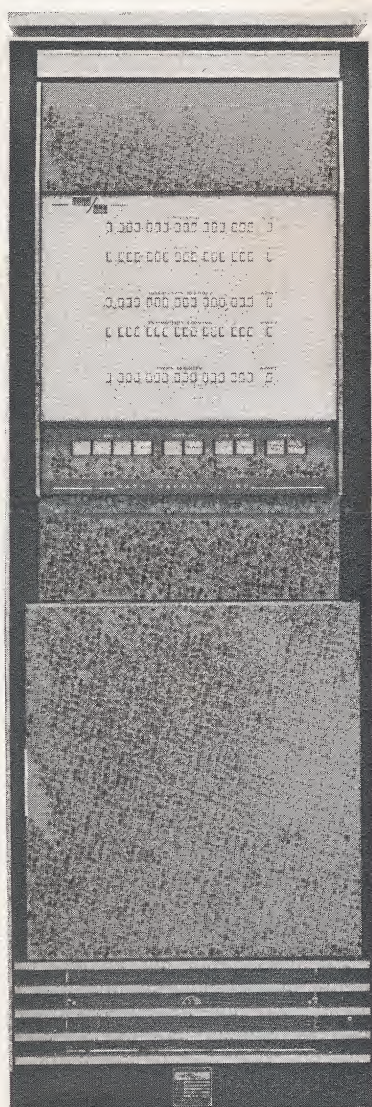
Model	Item
620-00	DATA 620 system computer, 16-bit word, 4096 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-01	DATA 620 system computer, 16-bit word, 8192 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt. .
620-04	DATA 620 system computer, 16-bit word, 2048 words of core memory, party line communication system. Power failure protect and interrupt, console interrupt.
620-19	Micro-control adapter.
620-19-1	Micro-Exec adapter and external control keyboard. Contains key for each micro-step and a timing sequence key.
620-30	Magnetic tape control unit and one transport. Includes assembly and disassembly register. IBM-compatible, operates at 45 ips. Dual density, 556 and 800 bpi.
620-41	Disc Memory Master Control Unit and one disc file up to 256,000 16-bit words of storage. 66-kc word transfer rate.
620-58	Paper tape reader and adapter. Reads at 300 ips. Reads 5, 7 or 8 level tape.
620-59	Paper tape punch and adapter. Punches at 60 cps. Punches 5, 7 or 8 level tape.
620-59-1	Paper tape system with common controller includes Models 620-58, 620-59.
620-60	First TTY Unit added to computer, ASR-33 with adapter. Reads at 10 cps, punches and types at 10 cps. Operates on-line or off-line.
620-70	Classroom display 4 ft. by 6 ft., Pulse Mode for instruction in computer technology.

DATA MACHINES, INC.

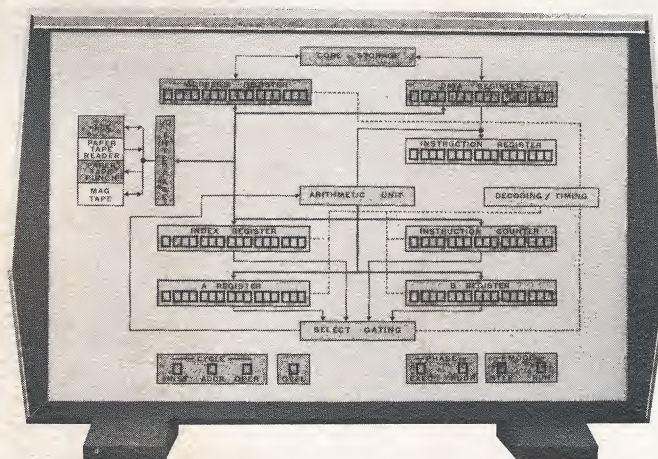
A DIVISION OF DECISION CONTROL, INC.

1590 Monrovia Ave. □ Newport Beach, California 92660 □ Tele: (714) 646-9371 □ TWX: (714) 642-1364

Computer



Classroom Display

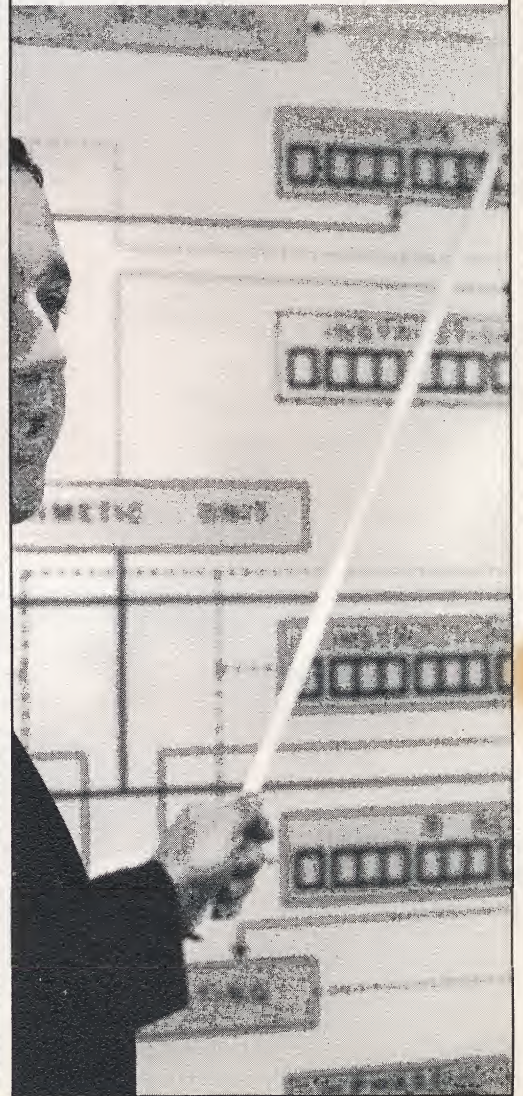
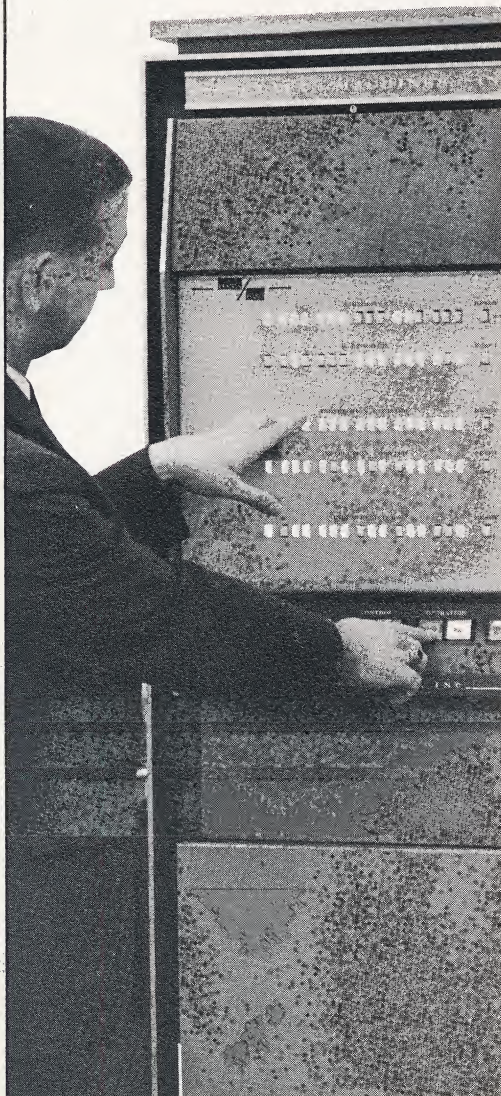


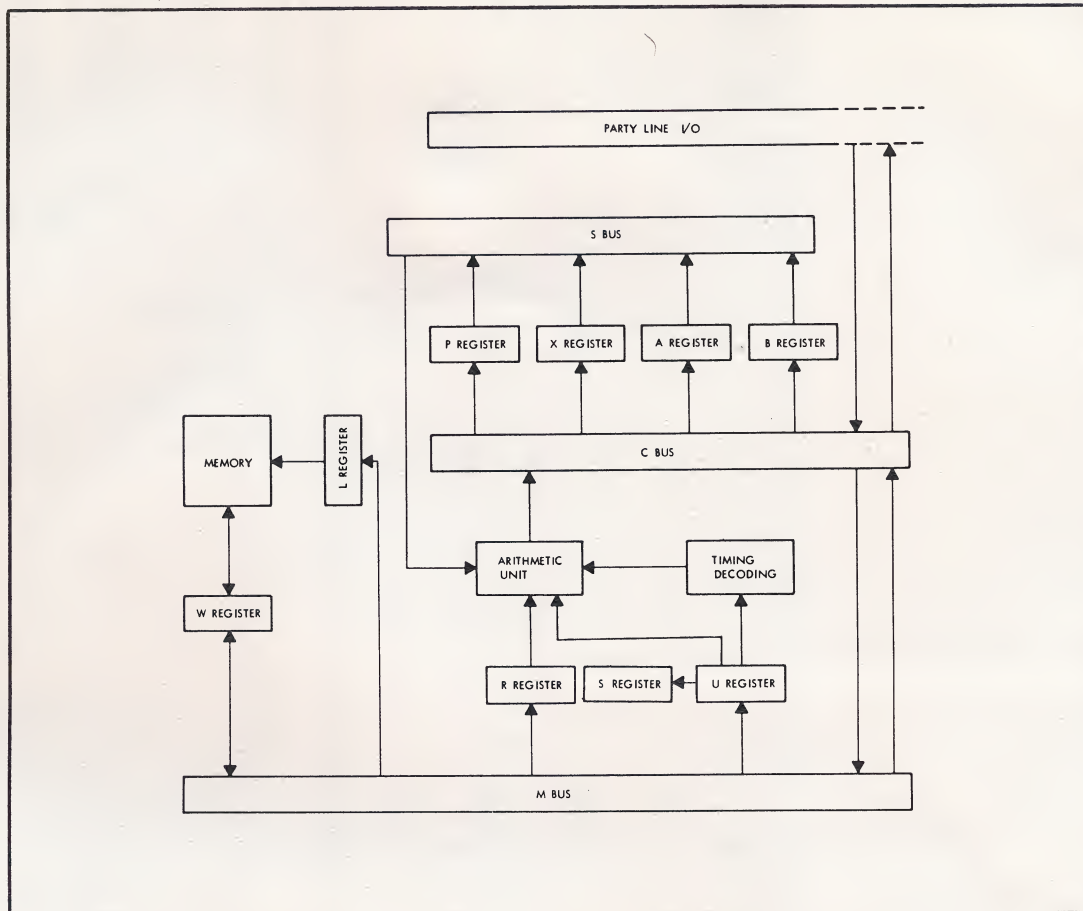
I/O Unit

The central processor is a general-purpose digital computer incorporating state-of-the-art designs. The instruction repertoire contains over 200 instructions; there are six addressing modes, the core memory is general purpose, and the input/output unit contains eight types of facilities. The comprehensiveness of the central processors' capabilities enable the instructor to demonstrate from simple to very complex operations. The processor can be operated in a pulse mode, step mode, repeat mode, or run mode.

All operational registers are displayed. The display lights are also data entry buttons. The data entry facility is automatically disconnected during the "RUN" mode to avoid accidental errors. The computer console provides both automatic and manual control. Contents of all operational registers are displayed on the console, and may be entered or modified manually. Program routines may be run continuously, in single operations or single steps, or in a pulse mode. The operating console has been optimized for convenience in preparing programs, inspecting operation, and verifying machine operations.

In the classroom, the display panel graphically shows data flow and illustrates typical computer organization with indicator lights; the panel demonstrates computer organization and information flow, and traces each instruction word from insertion through execution. Flow paths between functional blocks are shown to aid in visualizing internal routing of information through the computer. The panel is designed for classroom viewing up to 30 feet, and is connected to the central processor by a 25-foot cable.





Computer Organization

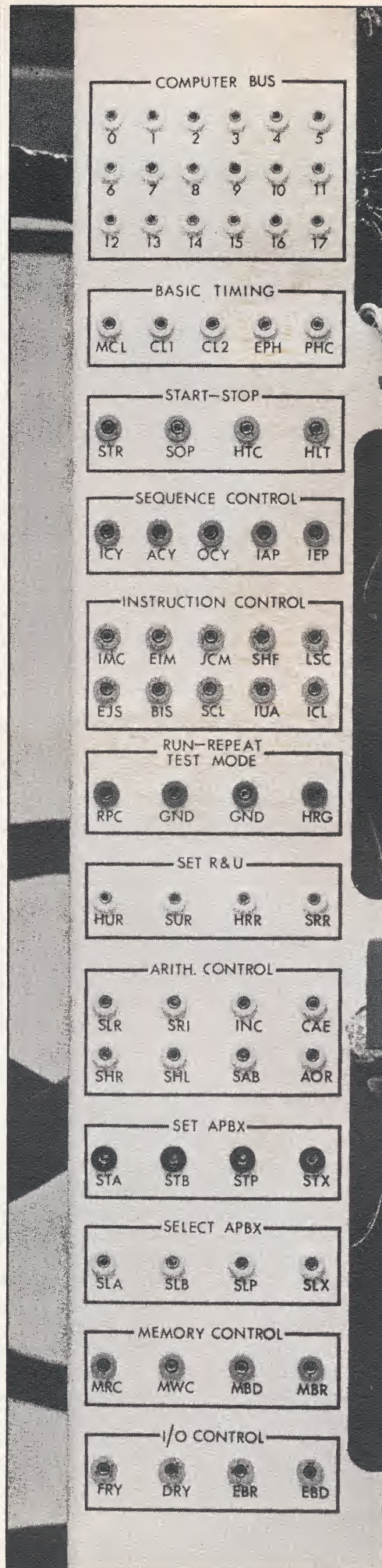
The 6F5 series general-purpose computer trainer is the result of a design philosophy which incorporates and contains nearly all the elements of present-day computers. It is oriented in every particular toward flexibility and modularity. The 6F5 is equally at home serving as a comprehensive training device, as well as a general-purpose stored-program computer. The 6F5 has a unique but simple internal organization which provides universal information routing. This uniqueness in design makes possible the implementation of complex algorithms with external control hardware (MICRO-EXEC).

To aid in visual demonstrations, a classroom display panel which pictorially shows data flow and illustrates computer operations and applications is an integral part of the digital computer trainer. The presence of the trainer in the classroom will enable the student to "see and do" as well as listen. Without the trainer at hand, much time may be spent attempting to describe or present a particular concept or area of the computer. But, if the trainer is in the classroom, it is possible to demonstrate and get the concept across in a very short time, and at the same time the level of student understanding will be increased.

Maintenance Panel

Observation of electrical waveforms is essential for locating specific malfunctioning components. When the book rack sections of the computer are opened, the test points on the maintenance panel may be used for convenient monitoring of all key signals within the computer. A maintenance panel is supplied with 74 test points, to observe the following:

- a. Computer bus
- b. Basic timing
- c. Start-stop
- d. Sequence control
- e. Instruction control
- f. Run-repeat test mode
- g. Set R & U
- h. Arithmetic Control
- i. Set APBX registers
- j. Select APBX registers
- k. Memory Control
- l. I/O Control



Specifications

TYPE	General-purpose digital computer trainer, magnetic core memory, binary, parallel, single-address, with bus organization.	
MEMORY	Magnetic Core, 16 bits (18 bits optional), 1.8 microseconds full cycle, 700 nanoseconds access time, 2048 words minimum, 4096 words standard, expandable in 4096 or 8192 word modules to 32,768 words, power failure protection (voltage and frequency), non-volatile. Each module with data and address register. Thermal overload protection.	
ARITHMETIC	Parallel, binary, fixed point, 2's complement.	
WORD LENGTH	16 bits standard; 18 bits optional.	
SPEED (FETCH & EXECUTE)	Add or Subtract	3.6 microseconds
	Multiply (optional	18.0 microseconds
	18 bits)	19.8 microseconds
	Divide (optional	18.0 to 25 microseconds
	18 bits)	19.8 to 28.8 microseconds
	Register change class	1.8 microseconds
	Input/Output—from A or B	3.6 microseconds
	from Memory	5.4 microseconds
OPERATIONAL REGISTERS	A-register—accumulator, input/output, 16/18 bits. B-register—double length accumulator, input/output, index register, 16/18 bits. X-register—index register, 16/18 bits. P-register—program counter, 16/18 bits.	
BUFFER REGISTERS	R-register—operand register, 16/18 bits. U-register—instruction register, 16/18 bits. S-register—shift register, 5 bits, operates with the U-register for executing shift instructions. L-register—memory address register, 15 bits, one L-register per memory module. W-register—memory word register, 16/18 bits, one W-register per memory module.	
CONTROL	Addressing Modes—Six Direct addressing to 2048 Relative to P register 512 words Index with X-register, hardware, does not add to execution time Index with B-register, hardware, does not add to execution time Multi-level indirect addressing Immediate Instruction Types—Four Single Word Double Word Generic Micro-command Instructions: 107 standard, over 128 macro instructions, plus 28 optional, consisting of: 3 Load 3 Store 5 Arithmetic (2 optional) 3 Logical 10 Jump 10 Jump and Mark 10 Execute 14 Immediate (2 optional)	

Instruction List

Type	Mnemonic	Description	Time Cycles
Load	LDA	Load A Register	2
	LDB	Load B Register	2
	LDX	Load X Register	2
Store	STA	Store A Register	2
	STB	Store B Register	2
	STX	Store X Register	2
Arithmetic	ADD	Add to A Register	2
	SUB	Subtract from A Register	2
	INR	Increment and Replace	3
	MUL*	Multiply B Register, Double Length	10
	DIV*	Divide AB Register, Double Length	10-14
Logical	ERA	Exclusive OR to A Register	2
	ORA	Inclusive OR to A Register	2
	ANA	And to A Register	2
Jump	JMP	Jump UNCONDITIONALLY	2
	JOF	Jump if Overflow SET	2
	JAN	Jump if Register NEGATIVE	2
	JAZ	Jump if A Register ZERO	2
	JAP	Jump if Register POSITIVE	2
	JSSI	Jump if the Sense Switch 1 SET	2
	JSS2	Jump if Sense Switch 2 is SET	2
	JSS3	Jump if Sense Switch 3 SET	2
	JXZ	Jump X Register ZERO	2
	JBZ	Jump B Register ZERO	2
Jump and Mark	JMPM	Jump UNCONDITIONALLY and Mark	2
	JOFM	Jump Overflow SET and Mark	2-3
	JANM	Jump A Register Negative and Mark	2-3
	JAZM	Jump A Register ZERO and Mark	2-3
	JAPM	Jump A Register Positive and Mark	2-3
	JS1M	Jump Sense Switch 1 SET and Mark	2-3
	JS2M	Jump Sense Switch 2 SET and Mark	2-3
	JS3M	Jump Sense Switch 3 SET and Mark	2-3
	JXZM	Jump X Register ZERO and Mark	2-3
	JBZM	Jump B Register Zero and Mark	2-3
Execute	XEC	UNCONDITIONAL Execute	2
	XOF	Execute Overflow SET	2
	XAN	Execute A Register NEGATIVE	2
	XAZ	Execute A Register ZERO	2
	XAP	Execute A Register POSITIVE	2
	XS1	Execute Sense Switch 1 SET	2
	XS2	Execute Sense Switch 2 SET	2
	XS3	Execute Sense Switch 3 SET	2
	XXZ	Execute X Register ZERO	2
	XBZ	Execute B Register ZERO	2
Immediate	LDAI	Load A Register Immediate	2
	LDBI	Load B Register Immediate	2
	LDXI	Load X Register Immediate	2
	STAI	Store A Register Immediate	2
	STBI	Store B Register Immediate	2
	STXI	Store X Register Immediate	2
	ADDI	Add to A Register Immediate	2
	SUBI	Subtract from A Register Immediate	2
	MULI*	Multiply, B Register Immediate	10
		Double Length	
	DIVI*	Divide AB Register Immediate	10-14
		Double Length	
	INRI	Increment and Replace Immediate	3
	ERAi	Exclusive OR to A Register Immediate	2
	ORAi	Inclusive OR to A Register Immediate	2
	ANAi	And to A Register Immediate	2
	EXC	External Control Function	1

	INRI	Increment and Replace Immediate	2
	ERAI	Exclusive OR to A Register Immediate	2
	ORAI	Inclusive OR to A Register Immediate	2
	ANAI	And to A Register Immediate	2
Input/Output	EXC	External Control Function	1
	CIA	Clear and Input to A Register	2
	CIB	Clear and Input to B Register	2
	CIAB	Clear and Input to A and B Registers	2
	INA	Input to A Register	2
	INB	Input to B Register	2
	INAB	Input to A and B Registers	2
	INM	Input to Memory	3
	OAR	Output A Register	2
	OBR	Output B Register	2
	OAB	Output OR or A and B Registers	2
	OTM	Output from Memory	3
	SEN	Sense Input/Output Lines	2-3
Register Change	IAR	Increment A Register	1
	DAR	Decrement B Register	1
	IBR	Increment A Register	1
	DBR	Decrement B Register	1
	IXR	Increment X Register	1
	DXR	Decrement X Register	1
	CPA	Complement A Register	1
	CPB	Complement B Register	1
	CPX	Complement X Register	1
	TAB	Transfer AR to B Register	1
	TBA	Transfer BR to A Register	1
	TAX	Transfer AR to X Register	1
	TBX	Transfer BR to X Register	1
	TXA	Transfer XR to A Register	1
	TXB	Transfer XR to B Register	1
	TZA	Transfer Zero to A Register	1
	TZB	Transfer Zero to B Register	1
	TZX	Transfer Zero to X Register	1
	AOVA	Add OV to A Register	1
	AOVB	Add OV to B Register	1
	AOVX	Add OV to X Register	1
	SOVA	Subtract OV from A Register	1
	SOVB	Subtract OV from B Register	1
	SOVX	Subtract OV from X Register	1
	SOV	Set Overflow	1
	ROV	Reset Overflow	1
Logical Shift	LSRA	Logical Shift Right AR k places	1 + .25 k
	LRLA	Logical Rotate Left AR k places	1 + .25 k
	LSRB	Logical Shift Right BR k places	1 + .25 k
	LRLB	Logical Rotate Left BR k places	1 + .25 k
	LLSR	Long Logical Shift Right k places	1 + .25 k
	LLRL	Long Logical Rotate Left k places	1 + .25 k
Arithmetic Shift	ASRA	Arithmetic Shift Right AR k places	1 + .25 k
	ASRB	Arithmetic Shift Right BR k places	1 + .25 k
	ASLA	Arithmetic Shift Left AR k places	1 + .25 k
	ASLB	Arithmetic Shift Left BR k places	1 + .25 k
	LASR	Long Arithmetic Shift Right k places	1 + .25 k
	LASL	Long Arithmetic Shift Left k places	1 + .25 k
Control	HLT	Halt	1
	NOP	No Operation	1

*Denotes optional instruction. Times given are for 16-bit computer.

Add 1 cycle for each level of indirect addressing.

SPECIFICATIONS (Cont.)

- 13 Input/Output
- 26 Register Change
- 6 Logical Shift
- 6 Arithmetic Shift
- 2 Control
- 6 Byte (optional)
- 14 Extended addressing (optional)
Over 128 micro-instructions

MICRO-EXEC (Optional)

Facility and hardware to construct a hardware program external to the DATA 620. Eliminates stored program memory accessing by use of hardware program.

Console

Display and data entry switches on all operational registers; 3 sense switches; manual interrupt; automatic load option; instruction repeat; single step; run; power on/off.

Maintenance Panel

Contains test points and jacks for: Computer Bus, Basic Timing, Start/Stop, Sequence Control, Instruction Control, Run-Repeat Test, Set R & U, Arithmetic Control, Set Registers, Select Registers, Memory & I/O Control.

INPUT/OUTPUT

Data Transfer

Four modes: Single word to/from memory (program control); single word to/from arithmetic registers (program control); Buffer Interlace Control (optional—up to 200,000 words/sec.) Direct Memory Access (optional—555,000 words/sec. max.)

I/O Party-Line Access (standard) over 200,000 word/sec.

Memory Party-Line Access (standard) to 555,000 words/sec.

External Control and Program Sense

Up to 512 external control lines, up to 512 external sense lines.

Interrupts

Power failure/thermal overload and console interrupts standard. Priority interrupts expandable in groups of eight (interrupt of interrupt), enable/disable and individual arm/disarm. Each interrupt line has unique memory destination address.

PHYSICAL

Dimensions

Main Processor (up to 8k and 18 bits)—26¼ inches high, 19 inches wide, 28 inches deep; memory power supply—5¼ inches high; logic power supply—5¼ inches high.

Access

Front: All chassis, drawer and/or page mounted for full front access.

Weight

400 lbs.

Power

500 watts, single phase, 115 ± 10V, 60 ± 2 cps. Power supplies are regulated. Additional regulation is not required under normal commercial power sources. A constant voltage ferroresonant transformer provides magnetic regulation of the —12V output. The +6V output is zener regulated.

Construction

Modular, logic pages unhinge and unplug. All drawers are connector coupled. Bit/slice packaging. Remote control panel (optional).

Expansion

Main processor contains provisions and space for all internal options and memory expansion to 8192 (16/18 bit) words. Peripheral controllers and special interfaces available in 7-inch drawers. Memory module book racks of 4096 and 8192 words available for expansion to 32,768 words (plug-in).

Installation

Mounts in standard 19 inch cabinet, no air conditioning, sub-flooring or special wiring and site preparation required.

Environments

0°C to 45°C; 0 to 90% relative humidity.

LOGIC AND SIGNALS

8 mc VersaLOGIC, 2.2 mc clock, logic levels 0V false, —12V true. Noise rejection 6V. Worst-case design.

SOFTWARE

Complete package, includes: Assembler, Library Subroutines, AID, Maintain, Diagnostics, and FORTRAN. Modular in construction, expandable for application orientation.

BUSINESS REPLY CARD

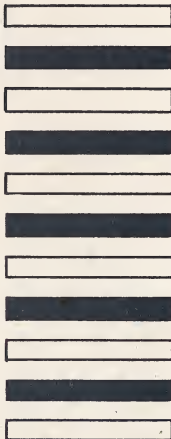
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FIRST CLASS
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Newport Beach
California



Announcing . . . The DATA 620 General Purpose Digital System Computer

SYSTEM FEATURES	PROCESSOR FEATURES	SOFTWARE & SERVICE
Micro-Exec. Party Line-I/O Packaging Flexibility Front Access Independent GP Memories Light Weight, Low Power Plug-In Field Expansion Six Types I/O Rack Mounting Compatible VersaLOGIC	16 or 18 Word Length Two Hardware Index Registers Nine Hardware Registers Universal Bus Structure 1.8 μ Second Memory Six Addressing Modes Direct Addressing to 2048 Memory Expansion to 32,768 Failure Protection System Control Panel Displays	Fortran in 4K Macro Assembler Program Analysis, AID Maintain Library Open Ended Training: Programming Training: Maintenance Field Support User Support

Gentlemen:

- ☐ I require additional information
- ☐ Have a DMI sales engineer contact me
- ☐ Please add my name to your mailing list

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